Amendments to the Specification:

Please replace the paragraph on page 5, starting at line 22 with the following new paragraph:

If the process, in block 113, determines that heuristics have been used and no test environment has been found, in block 111, then the process determines that a test environment cannot be determined for the targeted internal portion. Thus, the process continues to block ~~19~~ 119 to target the next internal portion.

Please replace the paragraph on page 9, starting at line 21 and continuing to page 9, line 4 with the following new paragraph:

Referring back to FIG. 1 and in particular to block 101, the process receives a RTL circuit description. FIG. 3 illustrates a functional RTL circuit represented as a hardware description language. From a hardware description language, such as WHDL or Verilog, each process is converted to an assignment decision diagram. For a combinational process and a sequential process of a finite state machine (FSM), the two processes are combined into one assignment decision diagram. FIG. 4 illustrates the assignment decision diagram of the RTL circuit description of FIG. 3. For example, the RTL statement 301 (FIG. 3) is represented by the read nodes A, B, operation node ~~63~~ 61, assignment decision node 41 and write node NEXT_F. Reset, APORT, BPORT, CPORT, DPORT, E and Reset represent primary inputs and Oport represents a primary output. NEXT_A, NEXT_B,

NEXT_C, NEXT_D, NEXT_F, NEXT_G, NEXT_O and NEXT_STATE are assignment targets. Current_state represents a state register, a storage unit.